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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/791,663

03/02/2004

Pierangelo Confalonieri

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7590

04/11/2005

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EXAMINER

NGUYEN, LINH V

ART UNIT

PAPER NUMBER

2819

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/791,663

Applicant(s)

CONFALONIERI ET AL.

Examiner

Linh V. Nguyen

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 March 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9,22-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-9 is/are allowed.
- 6) ☒ Claim(s) 22-24 is/are rejected.
- 7) ☒ Claim(s) 25 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 March 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 7/19/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. This office action is in response to electing of claims from applicant filed on 03/08/05. Claims 1 – 9, and 22 –25 are elected for examination. Claims 10 – 21 are canceled.

#### ***Priority***

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in EPO on 03/14/03. It is noted, however, that applicant has not filed a certified copy of the 03425160.3 application as required by 35 U.S.C. 119(b).

#### ***Drawings***

3. Figure 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 21 - 24 are rejected under 35 U.S.C. 102(a) as being anticipate by Fig. 2 of Applicant Admitted Prior Art (AAPA).

Regarding claim 22, under background, on page 4 of applicant's specification disclosing a circuit (Fig. 2), comprising: a more significant bit converter (OPA2) having an analog voltage output (Vout) indicative of a more significant bit portion of an input digital signal (Vin); a less significant bit converter (MD0, MD1, MD2) having an analog current output indicative of less significant bit portion of the input digital signal (Page 5 lines 5 – 8); a summation circuit (N2) including a first input terminal (terminal of N2 connected to the left terminal of R1') coupled to the analog voltage output (Vout) and a second input terminal (terminal of N2 connected to the top terminal of R2'); and a

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feedback path (IL) coupled between the second input terminal (terminal of N2 connected to R2') and an output (IL) of the summation circuit (N2) and connected to the analog current output (SD2, SD1, SD0); wherein the less significant bit converter comprises; a first plurality of current generators (MD1, MD2); a second plurality of current generators (M3, MD0); and a selection circuit (DEC – 9Bit, Transcod-3Bit) that selectively (SD<2 : 0>) one or more of the first plurality of current generators (MD1, MD2) to the analog current output, or alternatively selectively (SD<2 : 0>) connects one or more of the second plurality of current generators (M3, MD0) to the analog current output, based at least in part on the less significant bit portion (LSB) of the input digital signal (D<2 : 0>).

Regarding claim 23, wherein the selection circuit (DEC – 9Bit, Transcod-3Bit) chooses between connection of the first and second plurality of current generators (SD2, SD1, SD0) based on the more significant bit portion of the input digital signal (D<11:3>).

Regarding claim 24 further comprising a current mirror circuit that mirrors (Page 4 lines 20 – 22), for use by the first and second plurality of current generators (M3, MD2, MD1, MD0), a current (I) which is flowing in the more significant bit (MSB) converter (OPA2).

### ***Allowable Subject Matter***

7. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the

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base claim and any intervening claims. The prior art does not teach wherein the feedback path comprises a first and second resistor connected to each other at a node to form a series voltage divider, the node in the feedback path being connected to the analog current output.

8. Claims 1 – 9 are allowed.

With respect to claim 1, in addition to other elements in the claim, the prior art does not teach a digital to analog converter having summation means for generating the analog quantity as the sum of the second voltage and the product of the first voltage multiplied by the predetermined coefficient, comprising a summation circuit with resistive feedback means including a voltage divider; and wherein the means for transforming the current into a second voltage comprises a conversion resistor that forms part of the voltage divider.

#### ***Contact Information***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are

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(703-872-9306) for regular communications and (703-872-9306) for After Final communications.

3/16/05

Linh Van Nguyen

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A handwritten signature in black ink, appearing to read 'Linh Van Nguyen', written in a cursive style.